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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/657,255	09/07/2000	Richard K. Sita	ATTI000141	1505

34456 7590 08/19/2003

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EXAMINER	
TRUJILLO, JAMES K	
ART UNIT	**PAPER NUMBER**
2185	5

DATE MAILED: 08/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/657,255	SITA ET AL.	
	Examiner	Art Unit	
	James K. Trujillo	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file: Preliminary Amendment A dated 1/2/01 and Change of Address dated 1/27/03.

2. Claims 1-24 are presented for examination.

Claim Objections

3. Claims 4-5, 13-15, 20-21, and 23 are objected to because of the following informalities:

a. As to claim 4:

i. on line 2 of the claim, "same level" should be deleted because it is not required.

ii. on lines 2-3 of the claim, "the clock distribution tree" should be changed to "the clock distribution network" because it currently lacks proper antecedent basis.

iii. on line 4 of the claim, "the tree" should be changed to "the network" because it currently lacks proper antecedent basis.

b. As to claim 5:

i. on line 4 of the claim, "first the device" should be changed to "the first device"

c. As to claim 13:

i. on lines 3-4 of the claim, "from external the first device at the first device" should be changed to "from a device external to the first device at the first device" for clarity.

d. As to claim 14:

i. on line 5 of the claim, "device a second" should be changed to "device to a second" for clarity.

e. As to claim 15:

i. on line 3 of the claim, "first clock edge" should be changed to "the first clock edge" for clarity.

ii. on line 8 of the claim, "data signal a the second device" should be changed to "data signal at the second device" for clarity.

f. As to claim 20:

i. on line 7 of the claim, "the second substrate" should be changed to "a second substrate" because it is the first recitation of a second substrate and currently lacks proper antecedent basis.

g. As to claim 21:

i. on line 11 of the claim, "a first input port" should be changed to "the first input port" to correspond to the independent claim, claim 20, which has a recitation of "a first input port" on line 2 of claim 20.

h. As to claim 23:

i. on line 13 of the claim, "the latching signal" should be changed to "a latching signal" because it is the first recitation of a latching signal and currently lacks proper antecedent basis.

For examination purposes the above changes are assumed.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1-6, 9-14, and 18-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Schnell, U.S. Patent 6,137,327.

6. Claims 15-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Li et al., U. S. Patent 6,446,180.

7. As to claim 1, Schnell teaches a method comprising the steps of:

a. receiving a first clock signal (FB_CLK at input of PD) [figure 5 and corresponding text];

b. providing a distributed clock signal (output of 110) to a clock distribution network having a plurality of endpoints (DQ-PADS) connected to a respective plurality of components (OCD's) [col. 5 lines 7-10]; and

c. modifying the distributed clock signal until a portion of the distributed clock signal (by 110) received at a first end point (DQ-Pads) of the plurality of endpoints is substantially synchronized to the first clock signal [col. 5 lines 11-23 and figure 5].

8. As to claim 2, Schnell taught the method according to claim 1 described above. Schnell further taught wherein the step of modifying includes providing a delayed representation of the distributed clock signal at the first endpoint [DQ_PC, figure 3]. Figure 3 shows the desired delayed representation of the distributed clock signal at the first endpoint.

9. As to claim 3, Schnell taught the method according to claim 1 described above. Schnell further taught wherein the step of modifying includes using a delay lock loop to modify the distributed clock signal [figure 5 and col. 4 lines 64-67].

10. As to claim 4, Schnell taught the method according to claim 3 described above. Schnell further taught wherein the first endpoint is at a same propagation level as a second endpoint (OCD_M) of the clock distribution tree, where the second endpoint drives a component (SSTL_IF) that is not part of the network [figure 5 and col. 5 lines 11-23].

11. As to claim 5, Schnell taught the method according to claim 4 described above. Schnell further taught providing a second clock signal (output of 110) from a first device (Delay Line Elements and Delay Control, 110) wherein the first clock signal is a delay representation of the second clock signal [figure 5 and col. 5 lines 24-29].

12. As to claim 9, it is rejected on the same basis as claim 5.

13. As to claim 10, it is rejected on the same basis as claim 6.

14. As to claim 13, Schnell teaches a method comprising the steps of:

a. providing a first clock signal from a first device (clock output 112 from device 110) [figure 5 and corresponding text];

b. receiving a representation of the first clock signal (REFCLK) from a device external to the first device at the first device [figure 5 corresponding text];

c. providing the representation of the first clock signal to a delay element (input to the Delay Line Elements and Delay Control 110, the delay elements are within 110) [figure 5 and corresponding text];

d. providing a delayed clock signal from the delay element (clock signal at output of 110) to a clock distribution tree (to OCD's and OCD_M), wherein the delayed clock signal is based upon the representation of the first clock signal (based on phase detector output which is determined by the first clock and a feedback clock), and the distribution tree includes a plurality of leaves that provide the delay clock to a respective plurality of components (to OCD's and OCD_M) [figure 5 and corresponding text];

e. providing a representation of the delayed clock signal from a first leaf (the path OCD_M to 106-108-102-118-PD) to the delay element, where the first leaf (OCD_M) is one of a plurality of leaves [figure 5 and corresponding text]; and

f. modifying the delayed clock signal provided by the delay element based upon the representation of the delayed clock signal from the first leaf (the amount of delay is controlled by the representation of the delayed clock signal and the reference clock) [figure 5 and corresponding text].

Specifically Schnell taught a method of receiving a clock signal. The clock signal is delayed and distributed to a clock distribution tree. The delay placed in the clock signal is based upon a delay of a leaf within the clock distribution tree.

15. As to claim 14, Schnell taught the method according to claim 13 described above. Schnell further taught wherein the step of modifying the delayed clock includes modifying the delayed clock by delaying the first clock by an amount approximately equal to a first propagation delay and a second propagation delay, wherein the first propagation delay is equal to a delay along a delay path from the first device (device 110) to a second device (device 106), and the second propagation delay is equal to a delay along a delay path from the second device (device 106) to the first device (110) [figure 5]. Schnell essentially teaches modifying the clock based on the delay throughout the entire clock path wherein the first propagation delay is from the first device (delay locked loop circuit) to a device. The second propagation delay is from the second device to the first device to generate a feedback clock, which completes the loop.

16. As to claim 18, Schnell taught an apparatus comprising:

a. a delay locked loop (delay line elements and delay control 110 along with PD) having a reference input (REFCLOCK from RCV 116), a feedback input (FB_CLK from output of 118) and a delayed reference output (output 112) [figure 5]; and

b. a distribution network (104) having a first node connected to the delayed reference output (at 112 into OCD DRV), and a plurality of end nodes (OCD's and OCD_M) connected to a respective plurality of components (DQ-Pads's), a first end node (beginning with OCD_M) of the plurality of end nodes connected to the feedback input

of the delay locked loop (via the SSTL_IF 106 – RCV 102 – Package RC_Delay_M 118 –PD and ending at delay locked loop 110), where the delay locked loop (the delay locked loop is interpreted to be the PD and the Delay line element and delay control 110) is one of the plurality of components [figure 5 and corresponding text].

17. As to claim 19, Schnell taught the apparatus according to claim 18 as described above. Schnell further taught wherein the distribution network (104) is a clock distribution network [figure 5]. Figure 5 depicts wherein the OCD-DLLCLK (delayed clock) is distributed to a plurality of endpoints.

18. As to claim 15, Li teaches a method comprising the steps of:

a. generating a first clock edge (from XCLK) at a first device (elements 150, 145, 155, 130) at a first time, wherein the first clock edge is associated with a first clock having a first period [figure 2 and related text];

b. receiving the fist clock edge at a second device (Address/Command Control Unit 105) at a second time, wherein the time between the first time and the second time is a first propagation delay [figure 2 and related text];

c. generating a data signal (BXA) at the second device at a third time in response to receiving the first clock edge, wherein the time between the second time and the third time is a second propagation delay (because the response must propagate through circuitry in 105 a second propagation delay is incurred) [figure 2 and related text];

d. receiving the data signal at a first component (Output latch 135) of the first device at a fourth time, wherein the time between the third time and the fourth time is a third propagation delay [figure 2 and related text];

e. providing a representation of the first clock to a delay component (delay locked loop 150) of the first device, wherein the representation of the first clock is approximately to the first clock delayed by an amount approximately equal to the sum of the first, second and third propagation delay (Li adjusts the delay according the delay seen by the data signal) [figure 2 and related text, especially col. 4 lines 6-26];

f. generating a distributed clock (DLLR0/DLLF0) from the delay component to drive a clock distribution network having a plurality of endpoints (Output latch 135 and DQ Delay model 155) [figure 2 and related text]; and

g. modifying the distributed clock until the representation of the distributed clock at the first endpoint is synchronized the representation of the first clock [col. 4 lines 6-26].

19. As to claim 16, Li taught the method according to claim 15, described above. Li further taught wherein the second device is a memory device [col. 3 lines 14-15].

20. As to claim 17, Li taught the method according to claim 15, described above. Li further taught wherein the first period is less than approximately 5 nanoseconds [col. 1 lines 28-31].

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 6-8, 11-12, 15-17 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schnell.

23. Claims 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li.

24. As to claim 6, Schnell taught the method according to claim 5 described above. Schnell does not expressly disclose wherein the step of providing the second clock signal includes providing the second clock signal to a propagation path *manufactured onto a first substrate, wherein the first substrate is not part of the first device (emphasis added).*

The applicant's specification does not disclose how having propagation path and devices on different substrates provides an advantage. The applicant's only state that different substrates are used. Schnell does not expressly limit his invention to working with any devices on any particular substrate.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Schnell by using the apparatus of Schnell in an environment wherein the step of providing the second clock signal includes providing the second clock signal to a propagation path manufactured onto a first substrate, wherein the first substrate is not part of the first device. An artisan would have been motivated to make the modification because it would allow the advantages of an improved delay lock loop which avoids deviations in delay due to *technology* and temperature effects taught by Schnell to be applied to such an environment [col. 2 lines 20-24].

25. As to claim 7, Schnell taught the method according to claim 6 described above. Schnell does not expressly disclose wherein the step of receiving the first clock signal (FB_CLK) includes receiving the first clock signal at the first device (Delay Line Elements and Delay Control, 110). Schnell shows receiving the first clock through another device (Phase Detector PD) prior to the first device. It would have been obvious to one of ordinary skill in the art to

modify Schnell by integrating the Phase Detector PD as part of the first device (Delay Line Elements and Delay Control, 110). An artisan would have been motivated to make the modification because integrating devices is well know in the art to reduce costs, improve reliability and increase speed of operation, all of which are desirable in Schnell. As shown in In re Larson 144 USPQ 247, making integral is not generally given patentable weight.

26. As to claim 8, it is rejected on the same basis as claim 7.

27. As to claim 11, it is rejected on the same basis as claim 8.

28. As to claim 12, it is rejected on the same basis as claim 8.

29. As to claim 20, Schnell taught the apparatus according to claim 18 as described above. Schnell further taught:

a. a first input port (RCV 116) having an output node (output of RCV 116) coupled to the reference input of the delayed locked loop, and an input node (VCLK), wherein the first input port, the distribution network, and the delayed locked loop are formed on a first substrate [col. 1 lines 42-48];

b. a first trace connected to the input node of the first input port (VCLK must be on a trace); and

c. a first output port having an output node coupled to the first trace wherein the output port is formed on the first substrate (the output node is logically coupled to the first trace) [figure 5].

Schnell discloses that prior teaches that the RCV receiving the clock, the network and OCD (off chip driver) are on the same chip and are therefore all on the same substrate [col. 1 lines 42-48].

Schnell does not expressly disclose wherein the first trace is formed on a second substrate, which is different than the first substrate. Schnell also does not expressly disclose a first output port having an output node coupled to the first trace wherein the output port is formed on the first substrate. Schnell discloses receiving a clock signal at a first input port from a first trace. The clock signal must be generated from some device having a first output port.

The applicant's specification does not disclose how having ports and traces on different substrates provides an advantage. The applicant's only state that different substrates are used. Schnell does not expressly limit his invention to working with any devices on any particular substrate.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Schnell by using the apparatus of Schnell in an environment where the first trace of Schnell is on a second substrate different than the first substrate and wherein the first output port is formed on the first substrate. An artisan would have been motivated to make the modification because it would allow the advantages of an improved delay lock loop which avoids deviations in delay due to *technology* and temperature effects taught by Schnell to be applied to such an environment [col. 2 lines 20-24].

30. As to claim 21, Schnell substantially taught the apparatus according to claim 20 as described above. Schnell further teaches:

a. a second output port having an output node (output of delay line elements and delay control) connected to a second trace (112);

b. a second device (delay line elements and delay control) having an input coupled to the second trace (at the output 112) and an output coupled to a third trace (logically coupled to VbCLK), wherein the second device is formed on a third substrate which is different from the second substrate and the third trace is formed on the second substrate; and

c. the first input port (RCV 116) having an input node connected to the third trace (VbCLK), and an output node connected to on of the plurality of components (delay line elements and delay control) [Figure 5];

Schnell does not expressly disclose wherein the second output port is formed on the first substrate, and the second trace is formed on the second substrate or wherein the second device is formed on a third substrate which is different from the second substrate and the third trace is formed on the second substrate.

The applicant's specification does not disclose how having ports and traces on different substrates provides an advantage or how they are novel. The applicant's only state that different substrates are used. Schnell does not expressly limit his invention to working with any devices on any particular substrate.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Schnell by using the apparatus of Schnell in an environment wherein the second output port is formed on the first substrate, and the second trace is formed on the second

substrate and wherein the second device is formed on a third substrate which is different from the second substrate and the third trace is formed on the second substrate. An artisan would have been motivated to make the modification because it would allow the advantages of an improved delay lock loop which avoids deviations in delay due to *technology* and temperature effects taught by Schnell to be applied to such an environment [col. 2 lines 20-24]. Further it is well known in the art to form devices, such as those disclosed by Schell, as separate devices on different substrates to isolate each device. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Schnell by forming the devices on different substrates.

31. As to claim 23, Li taught a method comprising the steps of:

a. providing a first clock signal from a first device (while not explicitly shown a first device must provide XCLK) [figure 2].

b. providing a second clock signal from the first device (to the delay locked loop 150);

c. receiving the second signal at a delay component (145) as a modified second clock (DLLCLK);

d. receiving a third signal at a storage component (Output Latch 135), in response to the first clock signal (via 105-115-125-130) wherein a latching signal is based upon the modified second clock signal (DLLR0/DLLF0 is based upon DLLCLK plus delay) and a previous latching signal from the delay component (used in the feedback loop to the delay locked loop to change the amount of delay) [figure 2 and related text];

e. latching the third signal at the storage component based upon the latching signal (DLLR0/DLLF0 is used to latch the third signal) [col. 4 lines 19-21].

Li does not expressly disclose wherein the first clock signal is transmitted over a first substrate to a second device, wherein the first substrate is not part of the first device or the second device; Li also does not expressly disclose wherein the second clock signal is transmitted over a second substrate, wherein the second substrate is not part of the first or the second device. In summary, Li teaches every limitation of claim 23 except the location of the devices used with respect to their substrates. It appears that because Li does not mention that the relationship of the substrates is crucial that his invention is independent of the location of the devices with respect to the substrates.

The applicant's specification does not disclose how having devices on different substrates provides an advantage or how they are novel. The applicant's only state that different substrates are used. Li does not expressly limit his invention to working with any devices on any particular substrate.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Li by using the apparatus of Li in an environment wherein the first clock signal is transmitted on a first substrate wherein the first substrate is not part of the first device and wherein the second clock signal is transmitted over a second substrate wherein the second substrate is not part of the first device or the second device. An artisan would have been motivated to make the modification because Li teaches his invention would reduce the phase delay in such an environment [col. 1 lines 33-46].

Further it is well known in the art to form devices, such as those disclosed by Li, as separate devices on different substrates to isolate each device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Schnell by forming the devices on different substrates.

32. As to claim 24, Li taught the method according to claim 23 disclosed above. Li further taught wherein the latching signal (DLLR0/DLLF0) is delayed from the modified signal (DLLCLK) by an amount approximately equal to a clock period of the modified second clock plus a delay time (delay adjusted by a feedback loop) between the latching signal being generated and the latching signal latching the third signal [figure 5 and col. 4 lines 22-37]. Figure 5 shows that DLLR0/DLLF0 is delayed from DLLCLK by about a clock period of DLLCLK plus an addition delay [col. 7 lines26-30].

Conclusion

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 6,150,863 to Conn et al. This patent teaches having adjustable delay for data lines to be synchronized with a clock signal based on feedback.

U.S. Pat. No. 5,870,445 to Farwell. This patent teaches delaying a clock signal to a clock tree using feedback.

U.S. Pat. No. 6,487,468 to Hassoun. This patent teaches delaying a clock signal to a plurality of devices based on feedback.

Japan Pat. No. JP411025030A to Nakase. This patent teaches a system that adjusts the period of latching.

Spagna, F.; "Phase locked loop using delay compensation techniques", Computers and Communications, 2000. Proceedings. ISCC 2000. Fifth IEEE Symposium on, 3-6 July

2000, Page(s): 417 -423. This paper teaches using a phase locked loop for delay compensation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (703) 308-6291. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

James Trujillo
August 14, 2003

THOMAS LEE
SUPERVISORY PATENT EXAMINER
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